REMARKS

These remarks are in response to the final Official Action mailed on February 12, 2002. Consequently, the present Amendment is being filed with a Request for Continued Examination (RCE). The Office Action rejected claims 35, 36, and 38-40 under 35 U.S.C. 112, first paragraph. In particular, the Office Action states maintains its rejection of the previous Office Action, namely that it fails to find support in the present application for "determining a likelihood that the memory device has a degraded state by applying each of a plurality of read voltages to a terminal of a first cell of the plurality of memory cells to generate a plurality of read results." This is respectfully submitted to be in error, as discussed below. Additionally, the filing of an RCE with this Amendment is being taken advantage of to add several new claims, as is also discussed below.

New Claims

New claims 45-51 are added by the present invention. As with the pending claims, these claims are drawn to the degradation or deterioration of the state of a memory device. More specifically, these new claims are drawn to the "scrubbing process" aspect of the present invention. These new claims lack the specific limitation, "determining a likelihood that the memory device has a degraded state by applying each of a plurality of read voltages to a terminal of a first cell of the plurality of memory cells to generate a plurality of read results", for which the Office Action fails to find support.

New claim 45 is as follows:

> 45. A method of operating a memory device having a plurality of memory cells, comprising:
>
> generating a first read voltage;
>
> applying said first read voltage to a terminal of a first cell of the plurality of memory cells;
>
> generating a first read result in response to said applying said first read voltage;
>
> generating a second read voltage;
>
> applying said second read voltage to said terminal of said first cell;
>
> generating a second read result in response to said applying said first read voltage; and
>
> determining from said first and second read results whether data storage of the memory device is deteriorated.

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The generating of a series of read voltages, including "scrub read high" (V_{SH}) and a "scrub read low" (V_{SH}) voltages, is described on page 15, line 24, to page 16, line 2. Step 901 of Figure 9 presents "applying said first read voltage to a terminal ..." (SET V_{PG} TO V_{SH}) and "generating a first read result in response..." (READ SECOND SECTOR). Similarly, step 903 of Figure 9 presents "applying said second read voltage to a terminal ..." (SET V_{PG} TO V_{SL}) and "generating a second read result in response..." (READ SECOND SECTOR). Steps 902 and 904 check the read results, "determining from said first and second read results whether data storage of the memory device is deteriorated", which corresponds to a NO. The scrubbing process is generally described in the Summary at page 6, line 23, to page 8, line 13.

Thus, it is respectfully submitted that new claim 45 is fully supported by the present application. Several claims dependent on claim 45 have also been added. Claim 46 add that the data is rewritten to the memory (step 905, Figure 9), with claim 47 further adding that this rewriting is performed using error correction code (ECC) logic (page 25, lines 10-17). Claim 48 specify that the process is part of a programming operation (step 808, Figure 8), and claim 49 specify that the process is part of a reading operation (page 25, line 27, to page 26, line 3). Claim 50 is drawn to the memory cells being multi-state memory cells (page 11, lines 3-14), and claim 51 is drawn to the embodiment of the present invention mainly discussed in the present application, namely floating gate transistors with the read voltages of Figure 10 applied to the control gate.

Therefore new claims 45-51 are believed both allowable and fully supported by the present application.

Claims Rejected Under 35 U.S.C. 112, First Paragraph

The present Office Action maintains its previous rejection of claims 35-36 and 38-40 under 35 U.S.C. 112, first paragraph. For the reasons given below, it respectfully submitted the present application provides support for the pending claims and that the rejection is consequently not well founded. In particular, the Office Action again fails to find support in the present application for the process of "determining a likelihood that the memory device has a degraded state by applying each of a plurality of read voltages to a terminal of a first cell of the plurality of memory cells to generate a plurality of read results." The Applicants believe that support for this process is clearly presented in the present application and are unclear as to what in particular is found lacking. In particular, the Office Action states that it

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fails to find "proper antecedent support" and it is unclear to what the "antecedent" is in reference.

In its Response to Arguments section, the Office Action refers only to the portion of the Applicants' previous Response discussing the support provided with respect to Figure 8. Although it is again believed that, as previously discussed, Figure 8 does supply adequate support, this is only one embodiment found in the present application. In particular, the Office Action appears to completely ignore the following discussion of support for this element given with respect to Figure 9 given in the previous response.

More specifically, as discussed above both in the previous Response and above with respect to the newly added claims, Figure 9 of the present application is a flow chart of an embodiment for performing a "scrub" operation which is an alternate embodiment for the process of "determining a likelihood..." and "applying each of a plurality of voltages...". This figure is described mainly between page 24, line 24, and page 26, line 3, of the present application.

The scrub operation is described on page 24, line 9, to page 25, line 22. Specifically, beginning on line 32 of page 24, this section states:

> In step 901, a control gate voltage V_{SH} ... is applied. The cells are read in step 902 to see if there is any error as determined by the ECC [error correction code] check. ... In step 903, the scrub operation is performed again ... with a control gate voltage V_{SL}... . The cells are read in step 904 to see if there is any error as determined by the ECC check. ... In the scrub operation, ...the test can be performed utilizing the ECC logic 416 of Fig. 5.

Thus it is respectfully submitted that support is supplied for "determining a likelihood that the memory device has a degraded state [if NO in step 902 or 904] by applying each of a plurality of read voltages [V_{SH} and V_{SL}] to a terminal [control gate] of a first cell of the plurality of memory cells to generate a plurality of read results [steps 901, 902 and steps 903, 904]."

Conclusion

Therefore, it is respectfully submitted that the present application fully supports the claimed subject matter and that a rejection under 35 U.S.C. 112, first paragraph, is not well founded, and that claims 35, 36, and 38-40 are allowable. Reconsideration of the Office Action's rejection of claims 35, 36, and 38-40, consideration of new claims 45-51, and a prompt declaration of the previously requested interference is respectfully requested. The undersigned will attempt to follow up this Amendment with a telephone call in order to discuss these rejections in case further clarification is needed. In the meantime, however, if

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the Examiner has any questions about this request, application, or response, a telephone call to the undersigned is invited.

EXPRESS MAIL LABEL NO:
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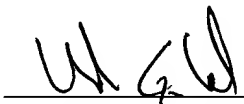
Respectfully submitted,



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5/9/02
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APPENDIX

Pending claims

35. A memory device comprising:

a plurality of memory cells, each of which is readable by application of a read voltage; and

means for determining a likelihood that the memory device has a degraded state by applying each of a plurality of read voltages to a terminal of a first cell of the plurality of memory cells to generate a plurality of read results.

36. The memory device of claim 35, wherein a group of the plurality of memory cells are arranged in a row that includes the cell, the memory device further comprising means for rewriting a previously stored value into each of the group of memory cells when the means for determining determines that the first cell has a degraded state.

(Claim 37 has been cancelled.)

38. The memory device of claim 35, wherein:

a group of the plurality of memory cells are arranged in a row that includes the first cell; and

the means for determining includes means for determining the likelihood by applying each of the plurality of read voltages when a write is performed on the group of memory cells.

39. The memory device of claim 35, wherein:

a group of the plurality of memory cells are arranged in a row that includes the first cell; and

the means for determining includes means for determining the likelihood by applying each of the plurality of read voltages when a read is performed on the group of memory cells.

40. The memory device of claim 35, wherein the terminal of the first cell is a control gate terminal of the first cell.

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(Claims 41-44 have been cancelled.)

45. A method of operating a memory device having a plurality of memory cells, comprising:

generating a first read voltage;

applying said first read voltage to a terminal of a first cell of the plurality of memory cells;

generating a first read result in response to said applying said first read voltage;

generating a second read voltage;

applying said second read voltage to said terminal of said first cell;

generating a second read result in response to said applying said first read voltage; and

determining from said first and second read results whether data storage of the memory device is deteriorated.

46. The method of claim 45, further comprising:

rewriting data to said plurality of memory cells in response to determining from said first and second read results that the data storage of the memory device is deteriorated.

47. The method of claim 46, wherein the data values written into said plurality of memory cells in said rewriting are determined based on error correction code (ECC).

48. The method of claim 45, wherein said method is part of a programming process.

49. The method of claim 45, wherein said method is part of a reading process.

50. The method of claim 45, wherein said memory cells are multi-state memory cells.

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51. The method of claim 45, wherein said memory cells are floating gate transistors and said terminal is a control gate.

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